Dual Mode Logic Gates in Coarse Grain Model for Power Switches

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Abstract: Power gating technology is used in power switches for reducing leakage power. Power switches are divided in to segments. Segments use DML gates. Dual mode logic gate use both dynamic and static operation. Faulty power switch is detected from segments hence achieve better diagnosis accuracy. The proposed diagnosis has been validated through number of ISCAS benchmarks. In the presence of temperature voltage and process variation, this DFT solution provides efficient testing of power switches; to achieve faster operation DML gates are used.

Keywords: DML (dual mode logic), power gating, DFT (design for test) power switches.

I. INTRODUCTION

Nowadays leakage current is a major problem in many digital circuits. Power gating technique reduces leakage power. By power down the logic block during idle mode for reduction of leakage power, power switches are usually implemented in two methods, they are fine grain or coarse grain. The main problem in fine grain method is high area overhead compared with coarse grain and also it is more sensitive to voltage, temperature, process variation changes.

There for coarse grain design style is most commonly used power switches can be implemented in two modes one is completely off mode other one is intermediate power off mode. This work fully concentrate on completely power off mode. DML means dual mode logic gate, there are two modes of operation static mode and dynamic mode. Static mode achieves low power dissipation and dynamic mode achieves faster operation. Static power dissipation occurs due to leakage current and sub threshold current. In DML which provide designer with very high level of flexibility. Different types of researches are done for DFT. In power switches possibly there are two types of faults are occurred, Stuck short, open test. Stuck open fault is due to drain or source of the transistor is disconnected showing faulty behaviour. Stuck short means there is a direct connection between VDD and ground. It can be detected by IDDQ testing. The power switches are divided in to segments. The delay test are used in both fine grain and coarse grain model. DFT solution suffers due to long discharging of transistor. In stuck at fault either logic 0 or logic 1 is present in the input and output lines. Single and multiple stuck at faults are occurred in logic circuits diagnosis is a systematic method for identifying faulty power switches. Fault means an error causing malfunction. Here only discuss about stuck at and stuck open fault. Be siding this fault bridging fault are exists. The rest of the paper is organized as II DML over view that gives basic idea of DML topology. III) analysis of fine and coarse grain. Which demonstrate power switches fault diagnosis. (IV) DML gate with power gating. Which demonstrate fast switching operation to find faulty behaviour of transistor) simulation result. This shows fault effects of power switches that is simulated using model sim software.

II. DML OVERVIEW

The digital circuits are the important blocks in integrated circuits. Hence the choice of cmos is sufficient. Two types of cmos I) pmos and II) nmos Static mode of circuit use both cmos and nmos devices.

A basic DML gate structure consists of static cmos gate and additional transistors M1 & M2 gate is connected to global clock signal. In this paper we suggest DML gate uses CMOS gate for the static operation. DML gate can be implemented in two types of methods type (a) and type (b). For static mode of operation high clock is applied for type A and low clock is applied for type B. To operate in dynamic mode two separate phases of operation is needed. 1) precharge and 2) evaluation. During precharge phase the output is charged in to VDD in type A and discharged in to ground in type B. During evaluation the output is evaluated according to the values of the gate input. The robustness in the dynamic mode is mainly achieved by the inherent active restorer that also enabling glitch sustaining, charge leakage and charge sharing. Dual mode logic can be operated in both static and dynamic mode. In dynamic precharge mode when clock is low the output node is precharged to VDD by the pmos transistor a standard cmos having both pull up and pull down network. The basic principle of this method for minimizing delays and achieve number of stages in the logical path containing cmos based dual mode logic gates fig (a) shows DML type A Fig (b) shows DML with type B. Both are used in power switch segments.

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III. ANALYSIS OF FINE GRAIN AND COARSE GRAIN

Power gating technique is used to reduce leakage current. There are two types of technique for power gating viz fine grain and coarse grain. In fine grain it in cooperates power switch within each standard logic cell with a control signal to switch on or off of the power supply of the cell. In coarse grain model a number of power switches are combined to feed back logic. The main drawback of fine grain is it utilizes maximum area compared with coarse grain. Fig 3 illustrates the fine grain design.

In this diagram control logic is used to control the test sequence. Multiplexers are used to enable standby mode or testing mode. Logic block help to save power by shutting unwanted blocks. The final output reaches at the NAND gate which shows fault response of the circuit.

IV. DML GATE WITH POWER GATING

In coarse grain model DML gate is implemented in segments mode selector select which mode of operation either static or dynamic. When they are alternatively switched to obtain better performance power gating technique reduces the leakage power of the static mode of operation. In dynamic mode faster switching performance is obtained.

V. COARSE GRAIN WITH DML

This paper demonstrates an efficient method for diagnosis for power switches. Power switches are divided in to segments. Number of power switches per segment is called segment size. In each segment DML topology is inserted. The proposed diagnosis method capitalizes on optimal segment size to determine the number of faulty power switches. The worst case of loss diagnosis accuracy is less than 12%. This is the first work in diagnosis of power switches with DML gate.
VI. ANALYSIS OF SEGMENT SIZE AND TEST FREQUENCY

In coarse grain DML model the control logic is used for controlling the test sequence. A multiplexer is used to enable test mode. The AND gate is used to control the discharging of transistor. The output of NAND gate shows fault response of the circuit.

The logic block consists of ISCAS bench marks designs that are synthesized using 90 nm gate libraries. The operating voltage used in this experiment is high. In coarse grain design style power switches are divided in to segments. And the number of power switches per segments has a tradeoff between area over head, test time and precision in identifying faulty transistor.

For a design shown in figure (5) segments consist of 5 power switches. We first stimulated test frequency and enable the test mode TE=1. D for controlling he discharging of transistor is set to zero. The power switches with DML is turned on and the fall time of the output of the NAND gate is observed when it reaches 20% of Vdd . This fall time is used to determine the test frequency. Hence we can determine maximum number of power switches per segment. Segment size varies from 5 to 30.

Another factor effecting diagnosis accuracy of power switches is that test frequency.

The number of detectable power switches is used to calculate diagnosis accuracy. When the number of undetected faulty switches increases diagnosis accuracy will be reduced. Another important parameter which effect is test frequency.

VII. DIAGNOSIS ALGORITHM

Input: (net list m,f1,f2,f3,f4)
Where m is the total number of segment size .
F1,f2,f3,f4 are the test frequencies
Output:Faulty segments with number of power switches
1.TE=1
// TE is test enable
2.FF1=f1;FF2=f2
// FF is the frequency at which segment fails and used to mdetermine the faulty power switches
3.D=1
// Enable discharge transistor
4. S_i=1
//m is the total number of segment.
i=1
//i points to the first segment
6. repeat
7. TF=f1
// TF is the test frequency
8. si=0,D=0
// Turn on all segments at a time.
9. if out==0 then
// si is fault free
10. Else
Use lower test frequencies.(f2,f3andf4)to determine the number of faulty power switches.
11. push (I,FF1,FF2)
// Push on stack failed segment and the number of faulty power switches
12. end if
13. Si=1; d=1
14. i++
15. Until i <= m
16. return

VIII. SIMULATION RESULT
By using model sim software the simulation results are verified. By using ISCAS benchmarks synthesized in 85 nm gate library. Simulation result is verified using test bench waveform. Under different test frequency are tested for better diagnosis accuracy.

IX. CONCLUSION
This work demonstrated an efficient diagnosis method to identify number faulty power switches in a logic circuit. The proposed method shows DML with coarse grain, it achieves high diagnosis accuracy compared with coarse grain. The diagnosis method is validated through number ISCAS bench marks. Experimental results at normal pressure, temperature and process variation 100% of accuracy obtained. Continued work in this paper including testing of power switches in conventional cmos gates.

REFERENCES