Low Power Programmable PRPG with NLFSR Based Test Pattern

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Abstract— The pseudorandom test pattern generator is used to generate the random test patterns and the patterns are needed to detect the faults in the circuit. This project describes a low power (LP) programmable pseudorandom test pattern generator (PRPG) and it has the capacity to produce the pseudorandom test patterns with desired toggling activities. The NLFSR (Non-linear feedback shift register) is used to implement the generator. The NLFSR is used to drive the phase shifter and allowing it to produce binary sequences with Pre-selected toggling (PRESTO) levels. The generator is controlled automatically and test vectors are combined with improved fault coverage. The test pattern generator is suited for Low power BIST applications. The obtained simulation results are used for industrial designs.

Keywords— BIST [Built In Self Test], PRPG [Pseudo Random Pattern Generator], NLFSR [Non-Linear Feedback Shift register], PRESTO [Pre-Selected Toggling activities].

I. INTRODUCTION

Testing is one of the most expensive parts of device. Manufacturing test should check each and every node in the circuit to ensure that it is not stuck [8]. To prove each node is fault free, the smallest sequences of test vectors are applied to the device under test. The number of test vectors for manufacturing test is reduced by good observability and controllability of nodes. In this project, we have proposed a new pseudorandom pattern generator for low power BIST applications. Generally, Scan is used to make testing of sequential circuits tractable. Current VLSI manufacturing processes suffer from larger defective parts ratio, partly due to numerous emerging defect types. While traditional fault models, such as the stuck at and transition delay fault models are still widely used, they have been shown to be inadequate to handle these new defects [8].

In general power dissipation of a system is higher in test mode than the normal mode. In scan mode each flipflops can be converted into a scan register by adding one extra multiplexer [2]. In normal mode the flipflops act as a normal memory elements. The extra power can cause problems such as instantaneous power that cause circuit damage, formation of hot spots, difficulty in performance verification and reduction of system lifetime and product yield.

Built-In Self-Test (BIST) is a self testing mechanism. That can be used to check the functionality of the device. It has been shown to be an effective design for testability (DFT) technique in which some on-chip test structure is used to test the digital circuit itself. Pseudo-random testing based on linear feedback shift registers (LFSR) is widely used because of its simplicity and effectiveness [7]. The feedback shift register is a type of digital oscillator. However this mechanism fails when a complex circuit often contains some hard-to-detect faults. At this case pseudo random test scheme usually requires long test time to reach satisfactory fault coverage. To overcome this problem, so many techniques have been proposed. Design for testability (DFT) refers to those design techniques that make test generation and test application cost-effective. Structured DFT involves adding extra logic and signals dedicated for test according to some procedure. The circuit has two modes, normal and test mode. The most commonly used structured methods are Scan and BIST. The NLFSR is used to generate pseudorandom sequences and it is used for various applications such as data compression error detection and correction, Testing and cryptography. The LFSR has linear complexity due to large number of stages [1].

LFSRs are simple, fast, and easy to implement in both, software and hardware. They are capable of generating pseudorandom sequences with the same uniform statistical distribution of 0’s and 1’s as in a truly random sequence [3][2]. However, they are not reliable because the structure of an n-bit LFSR can be easily deduced by observing 2n consecutive bit of its sequence. One solution to this problem is to feed the outputs of several parallel LFSRs into a non-linear Boolean function to form a combination generator. The generator main aim is to reduce switching activity.

The test power can be reduced by minimizing the number of transitions in memory elements. The low transition generators are combined with a 3- weight pseudorandom test pattern generator to reduce the switching activity of BIST[8]. Weighted random patterns have been used to reduce the test length for combinational circuits. The input sequences probabilities are properly selected to increase the efficiency of test vectors in detecting faults resulting in reduced test time.

II. PRPG[PSEUDORANDOM TEST PATTERN GENERATOR]

Pseudorandom test patterns are random in nature and it replaces original random sequences. Pseudorandom test pattern generation is a simplest method of creating tests. It uses pseudorandom number generator to generate test vectors and relies on logic simulation to compute good machine
results and fault simulation to calculate the fault coverage of the generated vectors.

A. NLFSR[Non-linear feedback shift register]
Non-linear feedback shift registers [NLFSR] are a generalization of linear feedback shift register [LFSR] in which the current state is a non-linear function of the previous state. In the Galois configuration the feedback can be applied to every bit and it decreases the propagation time and increasing the throughput. The feedback shift register is a type of digital oscillator. There are numerous applications of NLFSR such as code generation, counting and sequence recognition (or) decoding.

Galois NLFSRs do not concatenate every tap to produce the new input (the XOR operation is done within the NLFSR and XOR gates are run in parallel, therefore the propagation times are reduced to that of one XOR rather than a whole chain), thus it is possible for each tap to be computed in parallel, increasing the speed of execution.

III. PRESTO GENERATOR
In this project, we propose a PRPG for LP BIST applications. The main of this generator is to reducing the switching activity during scan loading with its preselected toggling (PRESTO) activities. It can assume a wide variety of configurations that allow a given scan chain to be driven either by a NLFSR based PRPG itself or by a constant value fixed for a given period of time. The PRESTO generator allows loading scan chains with pattern saving low transition counts, and thus significantly reduced power dissipation, and it also enables fully automated selection of its controls such that the resultant desired test patterns feature, user-defined toggling rates. The flexible programming can be further used to produce tests superior to conventional pseudorandom vectors with respect to a resultant fault-coverage-to-test-pattern-count ratio.

A. Block Diagram
Fig.2 shows the block diagram of PRESTO GENERATOR. An n-bit PRPG is connected with the Phase shifter to produce the pseudorandom sequences. The PRPG can be implemented with NLFSR. The NLFSR is used to produce the test pattern sequences in a random order. The n-hold latches are placed in front of the phase shifter and the toggle control registers are used to control each latches. If the inputs are enabled means the data are going from PRPG to the Phase shifter then it is said to be in toggle mode. When the latch is disabled the captured bits are stored for a number clock cycles and the constant data are injected to the phase shifter. Now it acts as in hold mode. The scan chains are in hold mode because the phase shifter output is produced by using the latches.

The Toggle control registers supervises the latches. If the values are between 0’s or 1’s. Where 1 indicates the latches in the Toggle mode and 0’s indicates the latches are in the Hold mode. The enable inputs are given to the shift register are produced in probabilistic fashion by using the PRPG with a programmable set of weights.

The Phase shifter output is given to the Circuit Under Test (CUT). In weighted pseudorandom test pattern generator, the distribution of 0s and 1s produced on the output lines is not uniform. The different parts of a circuit may be tested more effectively than other parts by pseudorandom patterns having different distributions. Once the weight of the signals are determined, the appropriate circuit can be designed to generate pseudorandom having the desired distributions.

B. Architecture
The basic operational principle of this method is shown in Fig.3. The shifting period of each and every test pattern is divided into alternating sequences of toggle and hold intervals. To move this generator between two states we use a T-type flip-flop that switches whenever there is a 1 on its data input. If the T-type flip-flop is set to 0 it enters into the Hold mode. All the latches are disabled temporarily regardless of the Toggle control register. The AND gates are inserted on the inputs are enabled means the data are going from PRPG to the scan chains.
To determine the generator state (either in toggle or hold) 4-bit hold and toggle registers are implemented in this architecture. The input of the T-flip-flop is changed to 1 to terminate either hold or toggle mode. The 2-input multiplexer is controlled by the T-flip-flop and it also controls the source of data routing from the generator. The weighted logic is used to produce the weighted pseudorandom signals. The four AND gates determines the weights producing 1’s with a probability of 0.5, 0.25, 0.125 and 0.0625 respectively.

The size (n) of the PRPG is given means, the switching code k, the average number (n_k) of 1s occurring in the toggle control register. Clearly, n_k = p_k x n. The average number of active chains a_k are determined for each value of n_k and the number is determined by the phase shifter and it also depends on the number of 1s in the toggle control register. Active scan chain A=(T X S)/50 where T=Desired level of toggling=Total number of scan chains. The additional scan chain are to be disabled by d_k=a_k-A. For each value of h_k and t_k the ratio r can be calculated to find the difference between actual and theoretical values.

D. Simulation Results
The approach is validated by experiments on five variety of scan architecture and it is used in five industrial designs with 128-bit NLFSR implementing a primitive polynomial \(x^{128} + x^{65} + x^{33} + x^{25} + x^{16} + x^{8} + 1\) and feeding the phase shifter with 10,000 test patterns. The NLFSR generate more number of random test patterns. The Patterns are generally fault simulated and detected faults are withdrawal from the list.

The number of scan chains, phase shifter, switching code, hold and toggle values are calculated automatically by using the size of PRPG. The test patterns are produced with desired toggling levels and the scan chains also balanced. The procedures are given in the following steps.

The probabilities for each switching code (K) must be determined and it is given to the phase shifter. The probabilistic values are P=0.5, P=0.25, P=0.625 P=0.125 and P=0.5625 for the switching code values K=1,2,3,4, and 5 respectively. The probability value (p_k) to enable the flip-flops are also calculated for each hold(h_k) and toggle(t_k) period and it can be obtained by h_k=t_k=1/p_k

Fig.5 shows the PRESTO generator waveform. The stuck at fault coverage increases with the increased switching activity. The switching activity is determined for each and every test pattern. The phase shifters are synthesized separately and then the switching activity is compared with the resultant toggling rates to achieve better performance.

The testbench waveform is shown in fig:6, the PRESTO generator and the NLFSR based pseudorandom test pattern are integrated in the design. The latches are designed in such a way that...

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way that it acts either in hold or toggle mode. The phase shifter output is produced by combining the three hold period values and it consumes low power for the operations. The power dissipations are reduced due to the weighted logic used to determine the weights of random signals.

**Fig. 5** PRESTO generator output

**Fig. 6** Test bench waveform

### E. Improved Fault Coverage

The higher fault coverage can be obtained with shorter test time. The NLFSR based pseudo random test pattern is modified by placing mapping logic between the output of PRPG and the inputs of circuit under test (CUT). The test patterns produced by the PRPG are transformed in a more deterministic manner. The toggle control registers are driven by the test data and the test patterns are produced with improved fault coverage. To improve the fault detection probabilities, the distribution of number of 1s in the toggle control register are to be determined.

### IV. CONCLUSIONS

In the project, the Low Power PRESTO generator scans Produce Pseudorandom test patterns with desired switching activities. The same features can also used to obtain the reliable fault coverage compared to the conventional pseudorandom test pattern generators and it still reducing the toggling rates down to desired levels. The automatic programmable features are used here to control the test pattern generator. It is a very attractive LP test method that allows trading-off test coverage, pattern counts and toggling rate in a flexible manner.

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