Ultra-low Power VLSI Design using Novel Leakage Reduction Technique

Krishna Kant¹ and Vijay Kumar Magraiya²

¹Department of Electronics and Communication Engineering, SRCEM Banmore, Morena, India
²Research scholar, Assistant Professor,

krishna.kant153@gmail.com
vijay.magraiya@gmail.com

Abstract— The modern portable devices require huge number of transistors to support several functionalities. Therefore, these devices demands ultra-low power designs as these devices also have limited battery size. The power consumption due to leakage i.e. static power consumption has become a critical issue which requires effective leakage reduction technique to reduce static power consumption. This paper explores different leakage reduction techniques and compares them. A new leakage reduction technique is proposed that provides significant reduction in leakage over existing techniques. The simulation results on Synopsys HSPIC shows that the proposed leakage reduction technique provides 10% reduction in leakage over the existing leakage reduction technique existing in the literature.

Keywords— Low Power Design, Leakage reduction, Integrated Circuits, VLSI.

I. INTRODUCTION

The large power requirement in the portable devices has become a severe challenge in modern VLSI design. Significant efforts have given to reduce power consumption in these devices. The device level approach such as scaling provides reduction in power consumption but scaling has reached to a point where other phenomenon such as process variations is becoming more severe. The addition circuitry required to mitigate the effect of process variation is becoming more costly in terms of area/power/delay over the gain due to scaling. Therefore, it requires circuit level techniques to reduce static power consumption due to leakage. Among the several leakage reduction techniques, some of the technique demands device modification i.e. demands change in the fabrication process whereas other technique such as circuit or architectural level demands modification in the existing circuit or architecture to reduce leakage current [4]. The device level techniques are costly and cannot be adopted for most of the design, whereas the circuit and architectural level techniques are very flexible and can be easily adopted.

The circuit level techniques achieve efficient leakage reduction in which additional circuit is added. The series connected transistors in the transistor stacking technique reduce the leakage current. In this technique the stacking causes increase in the source voltage that reduces gate-to-source, drain-to-source and create a body-bias. Different techniques like dual-threshold and multi-threshold reduce leakage as reported in [6], which require leakage reduction by adopting low threshold transistors for critical path and high threshold transistors for non-critical path to avoid increase in delay. Similarly, new approaches such as LECTOR [7], ONOFIC, super cutoff etc have also shown as fine approach to reduce leakage current. The LECTOR technique uses two extra transistors in series between pull-up and pull-down network whereas ONOFIC technique uses parallel connected nMOS and pMOS transistors between pull-up and pull-down network. The super cutoff technique which is reported in [8] uses one pMOS transistor to gate leakage current and biased in supper cutoff condition. Although, supper cutoff technique reduces leakage by significant amount, the variable bias requirement increases its complexity and decreases it usage.

The paper explores different leakage reduction techniques in details and does the comparative analysis. Further, a novel leakage reduction technique that reduces leakage significantly without much overhead in power/area and performance is proposed. The simulation results show that proposed approach of leakage reduction provides significant reduction in leakage current over the existing technique is discussed in the later part of this paper. Finally conclusion of the proposed and existing leakage reduction technique is drawn in the last.

II. SOURCES OF LEAKAGE AND DISTINCT LEAKAGE REDUCTION APPROACHES

Significant efforts have been devoted to reduce the leakage within the device. The first subsection shows source of leakage in CMOS circuit then explanation on the different leakage reduction Technique.

2.1 Sources of Leakage

The leakage current [9] within a MOS can be expressed by the equation 1 given below.

\[ I_{\text{leak}} = I_{\text{sub}} + I_{\text{gate}} + I_{\text{BTBT}} + I_{\text{GIDL}} \]  

(1)

Sub-nanometer an MOS device having six major sources of leakage as shown in Fig. 1.

![Fig. 1: Sources of leakage in a transistor](image)

In the Fig. 1, \( I_1 \) is the reverse bias pn-junction leakage current whereas \( I_2 \) is the sub-threshold leakage. \( I_2 \) current drain-to-
source current flows while the gate is biased below threshold voltage. \( I_3 \) is the oxide tunneling current which arises due to large electric field and can be overcome by considering high-K material. \( I_4 \) represents leakage due to hot carrier injection whereas \( I_5 \) is gate induced drain leakage. Finally, the \( I_6 \) represent punch through current which is excessive and may burn out the transistor.

### 2.2 Leakage Reduction Techniques

This section details different leakage reduction techniques.

#### 2.2.1 Dual Threshold Approach

In this approach uses two types threshold voltage for non-critical path is high voltage [10] whereas low voltage for critical path in transistor as shown in Fig. 2. The higher threshold on non-critical path allows lower leakage of the circuit where lower threshold in the critical path reduces the delay of the design. Thus dual threshold approach provides low leakage without changing performance of the design.

![Fig. 2 Critical path with dark dots](image)

The higher fabrication cost of dual threshold transistors is major limitation of the dual threshold technique. Increasing complexity implementation method in dual threshold is not commonly employed.

#### 2.2.2 ONOFIC Technique

The ONOFIC technique [4] as shown in Fig. 3 is a circuit level approach and uses single threshold to minimize leakage current. The ONOFIC technique turns ON/OFF the summation transistor such that it reduces leakage current significantly without affecting the performance of the circuit. The power consumption reduces corresponding reduces leakage significantly without affecting the performance of the circuit. Moreover in this technique as body terminal of the both NMOS and PMOS are in connected to Vdd and Gnd respectively it increases the stacking effects and reduces leakage current. The PMOS/NMOS transistors must be in cut-off or in linear mode depending on the output logic.

![Fig. 3 ONOFIC approach of leakage reduction](image)

The presence techniques make reduction in leakage at the cost of large area overhead.

#### 2.2.3 Transistor Stacking

When two or more transistor in series is in off condition then sub-threshold current in the transistor reduces significantly [5]. In this condition, source voltage of the stacked transistor increases that reduces, gate-to-source (\( V_{GS} \)) voltage, drain-to-source (\( V_{DS} \)) voltage and increases the body reverse biasing voltage (\( V_{BS} \)) as shown in Fig. 4.

![Fig. 4 Illustration of transistor stacking](image)

Significant reductions in the leakage current in all these effects result are done by the researchers. To further the reduce leakage, more number of the series connected transistor are applied the input that made them turn-off. This technique reduction technique is sometimes called as forced stack technique.

#### 2.2.4 Body Biasing Approach

This technique uses the substrate biasing to minimize the leakage current as shown in Fig. 5. The threshold voltage increases corresponding increase the reverse biasing of body bias which in turn reduces the leakage current [11-12].
Thus, the whole design maintain significantly reduced leakage through keeping the lower threshold in critical path while the high reverse bias in the non-critical path to reduces leakage. The extra additional substrate bias circuit generates probably body bias voltage for both PMOS and NMOS when the logic circuit works in the standby or active mode. The reverse body biasing in the standby mode increases resistance of the leakage path thus minimize leakage current mainly. The threshold voltage of the device depends on body to source voltage. Threshold voltage depends according to the relation given in Eq. 1

\[ \Delta V_{th} = \gamma V_{SB} \]

where, \( \gamma \) is the body bias coefficient.

2.2.5 Super Cut-off Technique

In this technique a sleep pMOS transistor is connected in super cut-off region [8] as shown in Fig. 6.

Subthreshold current reduces exponentially with increasing gate to source voltage of sleep transistor.

2.2.6 LECTOR Technique

The LECTOR [7] approach uses two transistors which are pinched as shown in Fig. 7.

In this technique, one controlling transistor controls the other LCT. The controlling transistors are in near cut-off thus reduces leakages current or improve resistance in the path of supply to ground. Similarly, this technique uses single threshold and is input pattern independent approach. The supply-ground path leakage current reduces due to using LECTOR technique which is concept of transistor stacking where controlling transistor are inserted. When one or more transistors are in cut-off mode then large resistance between is seen corresponding large leakage reduction. This technique reduces leakage current mainly in both standby and active modes.

In order to reduce leakage within limited area/power overhead we provide a novel leakage reduction technique which is discussed in the next section.

III. PROPOSED LEAKAGE REDUCTION TECHNIQUE

The proposed technique as shown in Fig. 8 is a circuit level technique utilizes single threshold logic to minimize leakage current. This technique mainly reduces standby and active mode of leakage current without impacting performance thus reduces dynamic and static power consumption. In this technique two transistor using of PMOS and NMOS each this is connected in series to reduce leakage. The proposed logic holds transistors in series connected as shown in Fig. 8.
In this technique distinct input patterns at the inserted transistors M1 and M2 give distinct control to the leakage current. Both the transistors are kept in cut-off mode in standby condition to reduce the leakage current whereas in normal active mode both are kept in ON conditions.

The results of simulation in the next section show the efficacy of the proposed technique over the existing leakage reduction approach.

IV. SIMULATION RESULTS AND ANALYSIS
This section discusses simulation environment and design metrics to compare proposed design over existing.

4.1 Simulation Environment
All the techniques of leakage reduction are first implemented in Tanner 14.1 with similar sizing of the transistors. The 3-input NAND gate is utilized as design for implementing leakage reduction approaches. From the schematic diagram, the netlist is created and simulated with 45nm technology PTM file using Hspice simulator from Synopsys. The all possible combination of the input patterns are implemented and corresponding leakage is computed and obtained.

4.2 Comparative Analysis
The simulation results of various leakage reduction techniques on 45 nm technology node are illustrated in Table 1. It can be seen from the simulation results that proposed technique provides less leakage over the existing. Further the power consumption of the proposed leakage reduction is small over the most of the existing architectures as shown in Fig. 9.

V. CONCLUSION
This paper shows the first concern of high leakage power consumption of modern portable devices by proposing novel leakage reduction technique. In this paper, we have first compared distinct leakage reduction approaches existing in the literature and the comparison is done by implementing and simulating these designs using Tanner and Hspice tool with 45nm technology node. The simulation results using 3-input NAND gate show that proposed technique minimize leakage current significantly over the existing techniques with large area, power and delay overhead.

REFERENCES


