Performance and Analysis of CLA with Sal Logic & Reversible Logic to Reduce the Overall Power Consumption

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Abstract - Low power design has become one of the primary focuses in both analogue and digital VLSI circuits. Digital sub threshold logic circuits can be used for applications in the ultra-low power end of the design spectrum, where performance is of secondary importance. A sub threshold digital circuit manages to satisfy the ultra-low power requirement because it uses the leakage current as its operating switching current. This minute leakage current, however, limits the maximum performance at which the sub threshold circuit can be operated. Sub-threshold CMOS theory is a technique which can reduce the power consumption to lower than threshold voltage specified and adiabatic logic circuit is a technique to reduce energy consumption by suppressing the voltage applied to the resistance of the circuit. This paper proposes that sub threshold adiabatic logic design implementation of carry look ahead adder. Many power consumption techniques have come in existence and with that the low power design is also achieved by scaling supply voltage, considering sub-threshold region in this region thereby obtaining a minimum energy consumption which also suits for low operating frequency. By using SAL logic to design 4-bit carry look ahead adder (CLA) and reduces the overall power dissipation. Results are evaluated through extensive simulations in 180nm CMOS technology using CADENCE VIRTUOSO TOOL at 180nm technology.

Keywords - Adiabatic logic, Carry look ahead adder (CLA), Sub-threshold Adiabatic logic (SAL), low power, leakage.

INTRODUCTION
Power consumption is rapidly becoming a limiting factor in integrated circuit technology as device sizes shrink. Applications such as wireless sensors, RFID tags, and similar devices have only a very small amount of power available to them, and must be designed to use a minimum of energy. Computer processors have massive amounts of power available, but can fail or become permanently damaged if the energy they dissipate causes severe heating. In an attempt to address these concerns, we have tested the effectiveness of two low-power techniques, sub-threshold biasing and adiabatic charging, in the design. The continuous growth of recent mobile and portable devices and applications has caused a tremendous thrust for low power circuit design. Various methods and techniques, such as voltage scaling, clock gating, etc. have been applied successfully in the medium power, medium performance region of the design spectrum for lower power consumption. Nevertheless, in some applications where ultra-low power consumption is the primary requirement and performance is of secondary importance, a more aggressive approach is warranted. Operating the transistors of a digital logic in the sub threshold region has recently been proposed to achieve ultra-low power consumption. A sub threshold digital circuit manages to satisfy the ultra-low power requirement because it uses the leakage current as its operating switching current. This minute leakage current, however, limits the maximum performance at which the sub threshold circuit can be operated. The sub threshold circuit is thus suitable for certain applications which do not require very high performance.
**ADIABATIC PRINCIPLE**-The operation of adiabatic logic gate is divided into two distinct stages: one stage is used for logic evaluation; the other stage is used to reset the gate output logic value. Both the stages utilize adiabatic switching principle. In the following section conventional switching and adiabatic switching analyzed in detail. Conventional Switching There are three major sources of power dissipation in digital CMOS circuits those are dynamic, short circuit and leakage power dissipation. The dominant component is dynamic power dissipation and is due to charging, discharging of load capacitance. The equivalent circuits of CMOS logic for charging and discharging.

**SUB-THRESHOLD BIASING**-The concept of sub-threshold is fairly simple to understand, though the physics behind it can be daunting. In traditional CMOS processes the voltage threshold is the value for which the transistor is off. If the voltage potential from the transistors drain to source is below the threshold voltage this concept of the device being off is still considered true. However, in reality the transistor still retains it on off abilities at these low levels, because the current doesn’t completely shut off, it is diminished exponentially. Though the transistor will not perform at the level it was designed for it will still operate similarly. We will show how our circuit performed with different VDD values set below the voltage threshold.

**CMOS BASED CARRY LOOK AHEAD ADDER**

Carry look-ahead uses a tree structure to parallelize carry generation. The tree structure is based on two intermediate signals the, "carry propagate" and the "carry generate". If the generate signal at a position is asserted, there is an unconditional carry out at that position, i.e. a carry is "generated" at that point. If the propagate is asserted, the carry out follows the carry in, i.e. a carry is "propagated" though that circuit. When units creating generate and propagate signals are combined into groups, like in Fig, the generate for the group is asserted if any unit has its generate asserted and all subsequent propagates are asserted. The group propagate asserted if all unit propagates are asserted. Most other arithmetic operations, e.g. multiplication and division are implemented using several add/subtract steps. Thus, improving the speed of addition will improve the speed of all other arithmetic operations. Accordingly, reducing the carry propagation delay of adders is of great importance. Different logic design approaches have been employed to overcome the carry propagation problem. One widely used approach employs the principle of carry look-ahead solves this problem by calculating the carry signals in advance, based on the input signals. This type of adder circuit is called as carry look-ahead adder (CLA adder). It is based on the fact that a carry signal will be generated in two cases:

1. when both bits $A_i$ and $B_i$ are 1, or
2. when one of the two bits is 1 and the carry-in (carry of the previous stage) is 1.

The carry-look ahead is a fast adder designed to minimize the delay caused by carry propagation in basic adders. It utilizes the fact that, at each bit position in the addition, it can be determined if a carry with be generated at that bit, or if a carry will be propagated.

To get more insight of operation, let us consider the following Boolean equations of the carry look ahead logic.

\[
\begin{align*}
\text{Pi} &= A_i \oplus B_i \\
\text{Gi} &= A_i \land B_i
\end{align*}
\]

Both carry propagate and generate signals depend only on the input bits and thus will be Valid after respective gate delays (XOR gate area and delay is far more than AND gate)

**SUB THRESHOLD ADIABATIC LOGIC WITH CLA DESIGN**
CLA Design

These structures check either the pull-up or the pull-down network of the static standard logic. For instance, to implement a NAND or a NOR gate, merely the pull-up network may be placed between the provision clock and also the output load capacitors, whereas an AND or an OR gate may be enforced using the pull-down network between the provision clock and also the output load capacitors. Just in case of a NAND structure, for each input combination except \( A = B = 1 \), the output node voltage can follow the provision clock closely, and that we get an approximate output wave form. Once \( A = B = 1 \) through parallel PMOS junction transistor, run currents can flow because the transistors can behave nearly as a relentless current supply.

A really touch of charge are keep across the load capacitor, i.e., rather than ground potential, terribly tiny voltage are across the output. The basic building block of 4-bit CLA is given in Fig which is also very similar to the conventional structure. Hence, we implemented the sum \( (S_i) \) in three stages to avoid delay mismatching with the carry generation. In SAL-based 4-bit CLA, every stage will be controlled by the supply clock. Like the conventional approach, the expression of the \( i^{th} \) sum and the \( (i+1)^{th} \) carry output.

Existing System

This novel approach is efficacious in low-speed operations where power consumption and longevity are the pivotal concerns instead of performance. The schematic and layout of a 4-bit carry look ahead adder (CLA) has been implemented to show the workability of the proposed logic. The effect of temperature and process parameter variations on sub threshold adiabatic logic-based 4-bit CLA has also been addressed separately. Post layout simulations show that sub threshold adiabatic units can save significant energy compared with a logically equivalent static CMOS implementation. Results are validated through extensive simulations in CMOS technology using CADENCE SPICE Spectra. CMOS logic gate design to implement the CLA. Energy recovery logic style has emerged as a promising approach in strong inversion regime, to reduce dynamic power consumption. The overall performance of the circuit is very low. Adiabatic style can be used efficaciously in a sub
threshold regime to make the circuit more energy efficient.

**PROPOSED SYSTEM**

SAL requires the main features of the adopted logic style, such as power dissipation, leakage current, impact of temperature variation, operating frequency. To implement a NAND or a NOR gate, simply the pull-up network can be placed between the supply clock and the output load capacitors.

To avoid delay mismatching with the carry generation, the transistor count will be almost half compared with the conventional CMOS logic design as in SAL basic logic gates. CMOS & SAL implementation of CLA to calculate the average power consumption. CAL used in SAL can be reduce the power in the circuit.

Reversible logic implementation of CLA to reduce the dynamic power and heat dissipation. Reversible computation arises from the desire to reduce heat dissipation. Reversible are circuits (gates) that have one-to-one mapping between vectors of inputs and outputs; thus the vector of input states can be always reconstructed from the vector of output states.

**SIMULATION RESULTS**

![Fig: Circuit For CLA Using SAL](image1)

![Fig: Output Waveform](image2)
CONCLUSION

SAL has been presented in this paper for the advance the ultralow power research. SAL saves considerable energy compared with the static conventional logic counterpart over a wide range of frequency. In particular, the impact of temperature variation on leakage dissipation, output swing, etc., has been discussed thoroughly in this paper. Hence, the predicted values of optimum frequency and optimum supply voltage almost match the simulated ones. Post layout simulations using CADENCE VIRTUOSO TOOL at 180nm technology. Spectra and the comparison with the static counterpart explain the workability of SAL. This proposed logic scheme can be used in future energy-saving embedded circuits and mainly for energy efficient devices where ultralow power and longevity are the pivotal issues.

FUTURE WORK

In future, using the PERES logic gate in reversible logic to reduce the overall power. Reversible logic are the circuits that have one-to-one mapping between vectors of inputs and output. It is used to reduce the power.

REFERENCES